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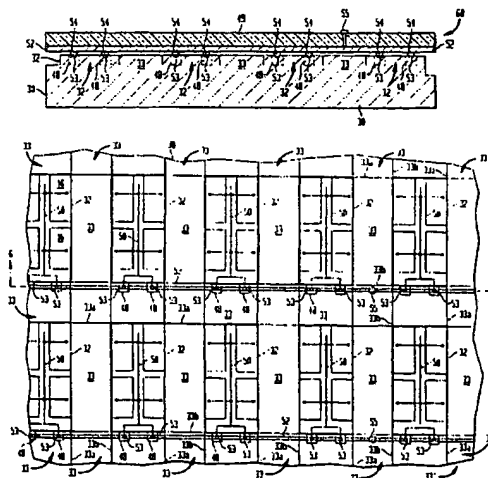
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(54) Title: SEMICONDUCTOR ARRANGEMENT



(57) Abstract: A semiconductor packaging arrangement, or module, includes a printed circuit board having an electrical interconnect thereon and a semiconductor package mounted to the printed circuit board. The semiconductor package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer. The fractional portion of the wafer has a plurality of electrical contacts electrically connected to the chips. The package also includes a dielectric member having an electrical conductor thereon. The electrical conductor are electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips with portions of the electrical conductor spanning the regions in the fractional portion of the wafer. A connector is provided for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

WO 01/99194 A3

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L23/528 H01L23/50 H01L21/66 H01L27/10 H01L21/82

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y		2,5
A		3,4
Y	US 6 055 655 A (MOMOHARA TOMOMI) 25 April 2000 (2000-04-25)	2,5
A	the whole document	1,3,4, 6-9

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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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